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1. Field of the Invention This invention relates to a method and system for semiconductor manufacturing. More particularly, the present invention relates to a method and system for manufacturing semiconductor devices having device layers formed from high-k dielectric material.

2. Description of the Related Art In semiconductor manufacturing, a substrate, such as a semiconductor wafer, is processed to form a large number of integrated circuit devices, each circuit device having multiple conductive layers. In a process called "front end of the line" (FEOL), device structures, such as transistors, are formed on a semiconductor wafer. In a process called "back end of the line" (BEOL), conductive lines are formed on the wafer to connect the individual circuit devices to form integrated circuits. The conductive lines are insulated from one another by layers of insulating material, such as SiO₂. Conductive lines are typically

formed by first depositing a thin conductive layer on a semiconductor substrate, patterning the conductive layer, and then etching the patterned conductive layer. Patterning the conductive layer typically involves depositing a photoresist layer on the conductive layer, irradiating the photoresist layer with light, developing the photoresist layer, etching the conductive layer, and then removing the photoresist layer. The conductive layer is typically composed of one or more conductive metals, such as tungsten, tungsten silicide, titanium, titanium nitride, copper, copper-tungsten

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